Hall Ticket Number:

Code No. : 22668

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

M.E. (E.C.E.) II-Semester Main Examinations, August-2023

Mixed signal IC Design

(Embedded Systems & VLSI Design)

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Compare analog and discrete time signals.	2	4	1	3
2.	What are the applications of op-amp w.r.t Mixed Signal IC Design.	2	1	1	3
3.	Define differential nonlinearity.	2	1	2	3
4.	Define aperture time.	2	1	2	3
5.	What is meant by absolute accuracy of analog to digital (A/D) converter?	2	1	3	3
6.	Define data acquisition time and latency.	2	1	3	3
7.	What is meant by aliasing w.r.t data converters?	2	1	4	3
8.	List the critical design specifications of A/D converters?	2	1	4	3
9.	What are the applications of phase-locked loops (PLL)?	2	4	5	3
10.	List different types of oscillators and what type of oscillator is suitable w.r.t. Mixed Signal IC Design.	2	1	5	3
	Part-B (5 × 8 = 40 Marks)				
11. a)	Draw the circuit and explain the working of three input switched capacitor integrator stage and give the expression for its output.	5	2	1	3
b)	Draw the diagram of an active-RC gain circuit and its equivalent switched capacitor circuit.	3	2	1	3
12. a)	Find the maximum sampling error for a S/H circuit that is sampling a sinusoidal input signal VIN = A Sin 2Πft. Where A is 2 V and f = 100 KHz. Assume that the aperture uncertainty is equal to 0.5 ns.	5	4	2	4
b)	Draw the circuit and explain the working of op-amp as Comparator.	3	2	2	3
13. a)	Draw the circuit and explain the working of a 6-bit flash A/D converter.	5	2	3	3
b)	Build the block diagrams for (i) Nyquist ADCs and (ii) over sampling ADCs.	3	3	3	3

Contd... 2

Code No. : 22668

14. a)	Build the diagram of a first-order sigma-delta modulator and explain its concept.	5	3	4	3
b)	Build the block diagram of an oversampling A/D converter.	3	3	4	3
15. a)	Build the diagram of a phase/frequency sequential phase detector based on NOR Gates and mention its concept.	5	3	5	3
b)	Build the block diagram of a ring oscillator realized using five digital inverters and mention the expression for its frequency of oscillation.	3	3	5	3
16. a)	Build the diagram of a switched-capacitor relaxation oscillator and explain its concept.	5	3	1	3
b)	Draw the diagram of basic sample and hold circuit and explain its concept.	3	2	2	3
17.	Answer any ***two*** of the following:				
a)	Draw the diagram of a 3-bit thermometer-based D/A Converter and explain its concept.	4	2	3	3
b)	Draw the block diagrams of peak detectors using (i) latched-comparator approach and (ii) continuous time approach.	4	2	4	3
c)	Draw the basic architecture of a phase-locked loop and explain its concept.	4	2	5	3

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	39%
iii)	Blooms Taxonomy Level – 3 & 4	41%

*****